New

MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2019/2020

DCS5158 – COMPUTER ARCHITECTURE

(DIT)

22 OCTOBER 2019
2.30 p.m. – 4.30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENT:

1. This question paper consists of **5** pages with **2** sections.
2. Answer **ALL** questions.
3. The distribution of marks for each question is given.
4. Write all your answers in the Answer Booklet provided

SECTION A: MULTIPLE CHOICE QUESTIONS (MCQ) (20 Marks)

Instruction: *Answer **ALL** the questions in this section and write your answers in the answer booklet provided.*

1. Which of the following structural component act as the internal storage to Central Processing Unit (CPU)?
   A. Control unit
   B. Memory cell
   C. Storage
   D. Registers

2. Which of the following register in CPU contains a word to be stored in memory or sent to the I/O unit, or is used to receive a word from memory or from the I/O unit?
   A. Memory buffer register (MBR)
   B. Instruction register (IR)
   C. Instruction buffer register (IBR)
   D. Memory address register (MAR)

3. Which of the following is a device that can store one bit of data; that is, the device can be in one of two stable states at any time?
   A. Gate
   B. Control unit
   C. Buffer
   D. Memory cell

4. Which of the following is the value of 1011.11_2 in decimal representation?
   A. 11.75_{10}
   B. 12.75_{10}
   C. 11.625_{10}
   D. 12.725_{10}

5. Which of the following is the normalized floating point format for 110.001_2?
   A. 1.10001×2^{-3}
   B. 1.10001×2^{-2}
   C. 1.10001×2^{3}
   D. 1.10001×2^{2}

6. In the instruction representation, the **Opcodes** are represented by abbreviations called _____.
   A. mnemonics
   B. operand
   C. fields
   D. elements

Continued...

7. In the following statement, identify *Y*.

> With Y, the address will specify which memory word or register contains not the operand but the address of the operand.

A. Direct addressing
B. Indirect addressing
C. Immediate addressing
D. Relative addressing

8. In the following statement, identify M.

> With M, it allows programs to address memory from a logical point of view, without regard to the amount of main memory physically available. When used, the address fields of machine instructions contain virtual addresses.

A. Volatile memory
B. Random Access Memory
C. Read Only Memory
D. Virtual Memory

9. From a user's point of view, the two most important characteristics of memory are capacity and performance. The three performance parameters are

I. Access time
II. Memory Cycle
III. Transfer Time
IV. Throughput

A. I, II and III
B. II, III and IV
C. I, II and IV
D. I, III and IV

10. It caries memory addresses from the processor to other components such as primary memory and input/output devices. What is the name of this bus?

A. Control Buses
B. Data Buses
C. Address Buses
D. Processor Buses

Continued...

SECTION B: STRUCTURED QUESTIONS (80 Marks)

Instruction: *Answer ALL the questions in this section and write your answers in the answer booklet provided.*

QUESTION 1 (20 Marks)

a) Given that the Program Counter (PC) contains 333, the address of the first instruction, and the partial list of opcodes with their meanings and original memory contents as shown in figures below.

i. Show the contents of the registers (Program Counter (PC), Accumulator (AC) and Instruction Register (IR) after execution of each instruction from memory address 333 to 337.

ii. Please Provide the memory contents of 888, 889, 88A and 88B after the final execution of fifth instruction.

[11 Marks]

Address	Content
333	1889
334	3888
335	288B
336	288A
337	4888
338	0000
...	...
888	0001
889	0002
88A	0003
88B	0004
...	...

Original memory contents

Instruction	Meaning
0000	Do nothing
0001	Load AC from memory
0010	Add to AC from memory
0011	Subtract memory from AC
0100	Store AC to memory

Partial list of opcodes

b) Perform the calculation of $-5_{10} - 3_{10}$ using 8-bits signed 2's complement binary numbers and convert your final answer in decimal. [4 Marks]

c) Perform the following conversions. All the necessary steps to obtain the answers must be shown.

i. Convert 775.23_8 to its hexadecimal equivalent. [3 Marks]
ii. Convert 2456_{10} to its hexadecimal equivalent. [2 Marks]

Continued...

QUESTION 2 (20 Marks)

a) Given the following expression,

$$C = [\ (T - (N + P * K)\ ) - (A * B)\ ]$$

i. Convert the expression C to postfix notation. [2 Marks]

ii. Write the expression C to the following machine instructions:

- One-address format [3 Marks]
- Two-address format [3 Marks]
- Three-address format [3 Marks]

iii. Draw the stack diagrams that illustrate the program execution for the zero address instruction. [5 Marks]

b) Memory system can be classifying according to their key characteristics such as method of accessing units of data. List **FOUR (4)** method of accessing units of data. [4 Marks]

Continued...

QUESTION 3 (20 Marks)

a) A computer system has a memory architecture consists of main memory of **64GB** and cache of **32768KB**. In order to perform an efficient mapping function, the main memory is arranged in blocks of **512 bytes**. (Assuming 1 KB = 1024B, 1MB = 1024KB, 1GB = 1024MB.)

Draw the address structures for different memory mapping functions as stated below. Indicate the fields and the number of bits required for each field.

i. **Direct Mapping** [6 Marks]
ii. **Thirty Two-Way Set Associative Mapping** [6 Marks]
iii. **Associative Mapping** [4 Marks]

b) Bus is a communication pathway connecting two or more devices. Differentiate between Internal Bus and External bus in the bus system. [4 Marks]

QUESTION 4 (20 Marks)

a) Briefly explain the operation of the following I/O techniques:
   I. Interrupt-driven I/O
   II. Direct Memory Access

[6 Marks]

b) Given **FIVE (5)** instructions where each instruction has **FIVE (5)** stages (FI, DI, CO, EI and WO) with delays of 3,3, 4, 5 and 2 seconds for each stage respectively.

i. Draw a timing diagram for instruction pipeline operation. [4 Marks]

ii. Calculate the **total processing time** and **throughput** for the implementation of pipelining and non-pipelining. [8 Marks]

iii. Calculate **the speedup factor** for the implementation of pipelining [2 Marks]

Note: Please write the formula that is appropriate to use and answers are up to 3 decimal places only]

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